Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A flash memory cell, comprising:
a substrate having a first opening and a second opening, wherein the second opening is formed on the bottom of the first opening and is narrower than the first opening but is deeper, as measured from the surface of the substrate, than the first opening;
a select gate on a sidewall of the first opening;
a floating gate on a sidewall of the second opening;
a gate dielectric layer between the select gate and the substrate as well as between the floating gate and the substrate;
a high-voltage doped region under the bottom of the second opening in the substrate; and
a source region formed beside the first opening in the substrate.

[c2] 2.The flash memory cell of claim 1, wherein the first opening and the second opening have round corners on their bottoms.

[c3] 3.The flash memory cell of claim 1, wherein the select gate and the floating gate are made of materials comprising polysilicon.

[c4] 4.The flash memory cell of claim 1, wherein the gate dielectric layer comprises a gate oxide layer.

[c5] 5.The flash memory cell of claim 1, wherein the high-voltage doped region is used simultaneously as a drain region and a control gate.

[c6] 6.The flash memory cell of claim 1, the flash memory cell further comprises insulating spacers on another sidewalls of the select gate and the floating gate.

[c7] 7.The flash memory cell of claim 1, the flash memory cell further comprises an insulating layer and a contact plug, wherein:
the insulating layer is form on the substrate and covers the select gate and the floating gate; and
the contact plug penetrates through the insulating layer and is electrically connected to the high-voltage doped region.

[c8] 8.The flash memory cell of claim 6, wherein the insulating spacer is made of materials comprising silicon nitride.

[c9] 9.A method of fabricating a flash memory cell, comprising the following steps:
providing a substrate;

forming a first opening and a second opening in the substrate, wherein the second opening is formed on the bottom of the first opening, the second opening is narrower but is deeper, as measured from the surface of the substrate, than the first opening;
forming a high-voltage doped region under the bottom of the second opening in the substrate;
forming a gate dielectric layer on the substrate in the first opening and the second opening;
forming a first conductive spacer on a sidewall of the first opening as a select gate, and forming a second conductive spacer on a sidewall of the second opening as a floating gate; and
forming a source region beside the first opening in the substrate.

[c10] 10.The method of fabricating a flash memory cell of claim 9, wherein the step of forming the first opening comprises:
forming a mask layer with the pattern of the first opening over the substrate; and
etching the substrate with the mask layer as mask to form the first opening.

[c11] 11.The method of fabricating a flash memory cell of claim 10, wherein the first opening has round corners on its bottom.

[c12] 12.The method of fabricating a flash memory cell of claim 10, wherein the step of forming the second opening comprises:
forming spacers on the sidewalls of the mask layer and the first opening; and
etching the substrate, with the mask layer and the spacers as mask, to form the second opening.

[c13] 13.The method of fabricating a flash memory cell of claim 12, wherein the second opening has round corners on its bottom.

[c14] 14.The method of fabricating a flash memory cell of claim 12, wherein the process to form the high-voltage doped region under the bottom of the second opening in the substrate comprises a step of ion implantation, with the mask layer and the spacer as mask, to the substrate.

[c15] 15.The method of fabricating a flash memory cell of claim 9, wherein the process to form the gate dielectric layer on the surface of the substrate in the first opening and the second opening comprises thermal oxidation.

[c16] 16.The method of fabricating a flash memory cell of claim 9, wherein the process to simultaneously form the first and the second conductive spacers comprises:
forming a conformal conductive layer on the substrate;

and

anisotropic etching the conformal conductive layer to form the first conductive spacer on the sidewalls of the first opening and the second opening.

[c17] 17.The method of fabricating a flash memory cell of claim 16, wherein the materials of the conformal conductive layer comprise polysilicon.

[c18] 18.The method of fabricating a flash memory cell of claim 9, the method further comprises:

forming an insulating layer on the substrate, where the insulating layer covers the select gate and the floating gate; and

forming a contact plug which penetrates through the insulating layer and is electrically connected with the high-voltage doped region.

[c19] 19. The method of fabricating a flash memory cell of claim 18, the method further comprises a step, before the formation of the insulating layer, to form an insulating spacer on another sidewalls of the select gate and the floating gate so as to protect the floating gate in the process of forming the contact plug.